

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Art Unit:	2825
Serial No:	Examiner:	Levin, Naum B.
Filed:	Conf. No.:	7058
For:		
Amir Alon		
10/091,934		
March 6, 2002		
An Interconnect-Aware Methodology		
For Integrated Circuit Design		

RESPONSE TO RESTRICTION / ELECTION REQUIREMENT

Mail Stop Non-Fee Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Amendment is filed in response to the Restriction/Election Requirement dated April 9, 2008 issued by the United States Patent and Trademark Office in connection with the above-identified Application. A response to the April 9, 2008 Office Action is due May 9, 2008.

Accordingly, this Amendment is being timely filed.

Applicants elect to prosecute claims 50-51 of Group II, drawn to an integrated circuit design using frequency domain analysis.

Claims 43-45, 47 and 49 of Group I, drawn to an integrated circuit design using time and frequency domain analysis.

While this election is made without traverse, Applicants reserve all rights in these non-elected claims, claims 43-45, 47 and 49, to file divisional and/or continuation patent applications.

If the Examiner has any questions or comments as to this response, the undersigned may be contacted at the address and telephone number below.

Please charge any fees associated with this paper to deposit account No. 09-0468.

Respectfully submitted,

By: /Suzanne Erez/
Suzanne Erez
Reg. No. 46,688
Phone No. (972) 4-829-6069

Date: 5 May 2008
IBM Corporation
Intellectual Property Law Dept.
P. O. Box 218
Yorktown Heights, New York 10598